REMARKS

Claims 1-20 are pending, of which claims 12-18 have been withdrawn from consideration. By this Amendment, claims 1 and 8 have been amended, and new claims 21 and 22 have been added to further set forth the subject matter of the present application. No new matter has been introduced.

Applicant respectfully submits the following comments regarding claims 1, 8, 21 and 22, as amended and added, which are not anticipated or rendered obvious by prior art of record.

The power supply wirings (VDD & VSS) in Fig. 5B of ***Fudanuki et al.*** (U.S. Patent No. 6,054,872, hereinafter "***Fudanuki***") are provided on a line disposed on the same vertical position in a planar pattern (see 8: 66 to 9: 9). The vertical position of the power supply wirings is as high as the height (H) of outside dimensions of respective cells (see 9: 36-41). Additionally, the power supply wirings (VDD/VSS) in Fig. 10B of ***Fudanuki*** are placed common to the upper and lower cell rows respectively (see 12: 45-50).

The present invention as now set forth in claims 1-11 and 19-22 is characterized by a structure which has no fixed wiring for commonly wiring between fundamental cells in a plane pattern where fundamental cells are formed. Particularly, no fixed wiring is placed in a hierarchy where fundamental cells are formed so that signal wiring can be flexibly designed.

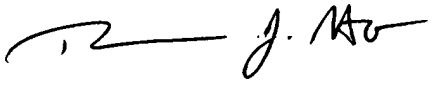
Applicant respectfully submits that this application is in condition for allowance and such action is earnestly solicited. If the Examiner believes that anything further is desirable in order to place this application in even better condition for allowance, the

Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below to schedule a personal or telephone interview to discuss any remaining issues.

In the event this paper is not considered to be timely filed, Applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn, PLLC



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Enclosures: Marked-Up Copy of Amended Claims

MARKED-UP OF AMENDED CLAIMS

1. (Twice Amended) A fundamental cell, used as a basic unit in layout of a semiconductor integrated circuit device [~~and being in a stage after metal wiring is formed~~], comprising:

no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells are form, and

connector terminals to be connected to upper wiring layers.

8. (Twice Amended) A semiconductor integrated circuit device, comprising:

a fundamental cell, used as a basic unit in layout [~~and being in a stage after metal wiring is formed~~], having no fixed wiring to be commonly wired between the basic units in a hierarchy where fundamental cells are form, and having connector terminals to be connected to upper wiring layers; and

upper wirings in predetermined wiring directions and in predetermined wiring widths both appropriately selected, for connecting, in the upper wiring layers, the corresponding connector terminals of the fundamental cell.